

7

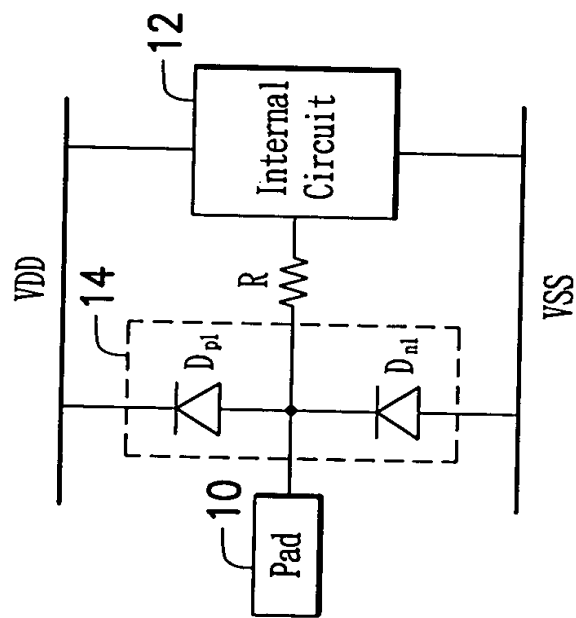


FIG. 1a (PRIOR ART)

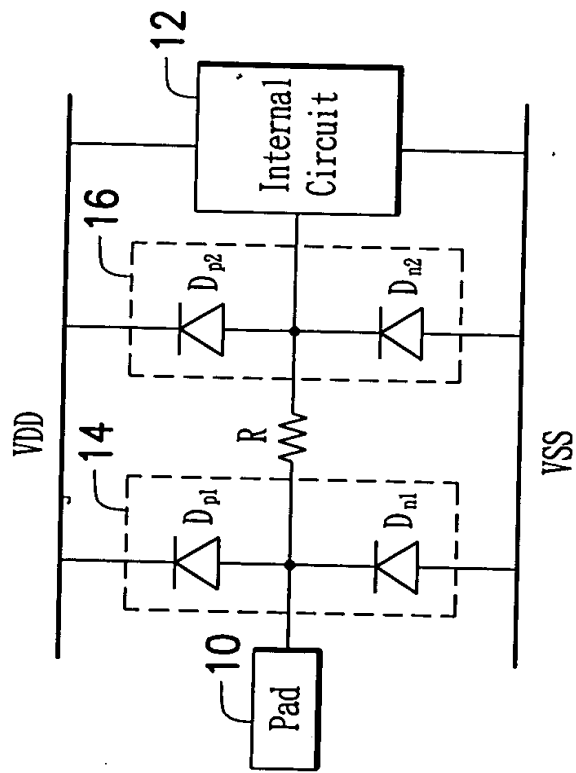


FIG. 1b (PRIOR ART)

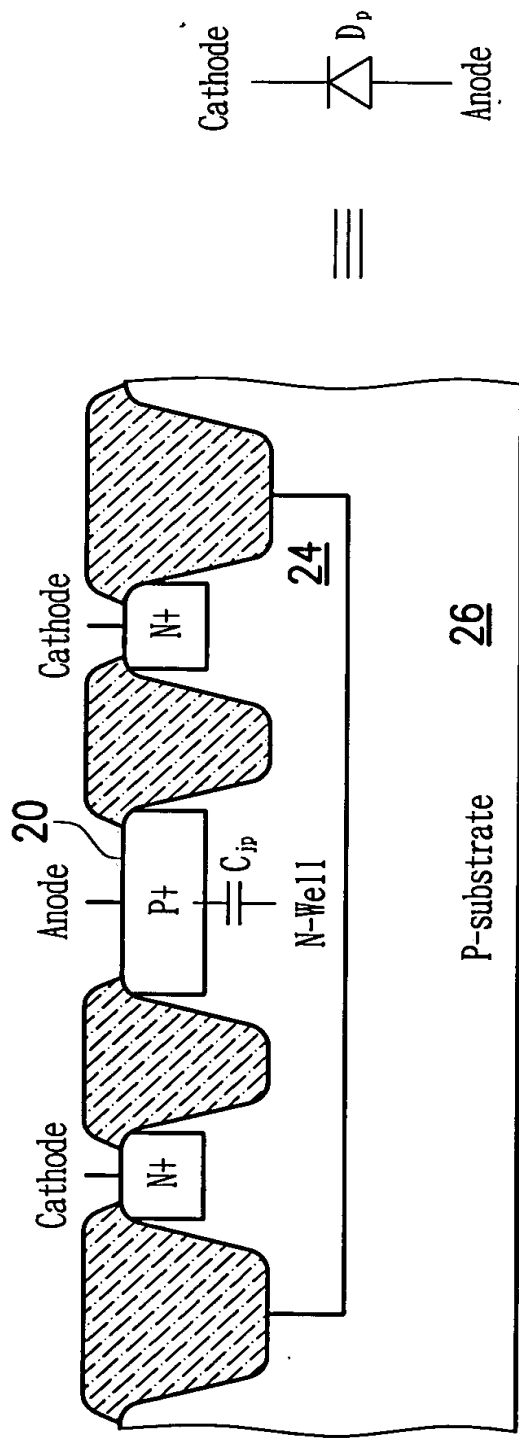


FIG. 2 (PRIOR ART)

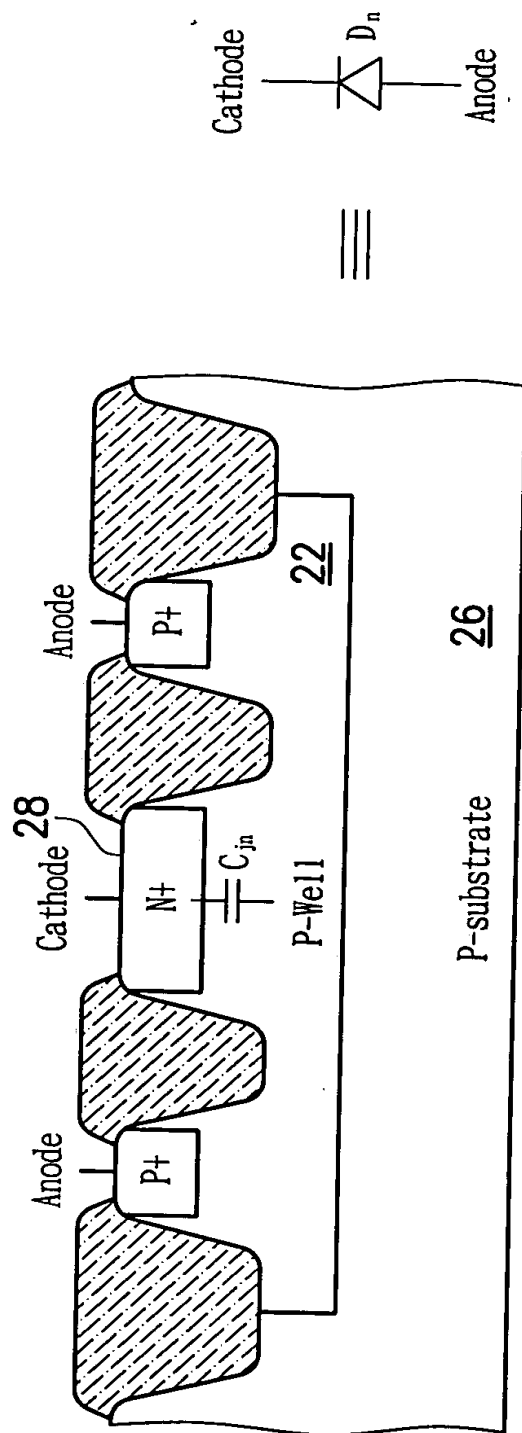


FIG. 3 (PRIOR ART)

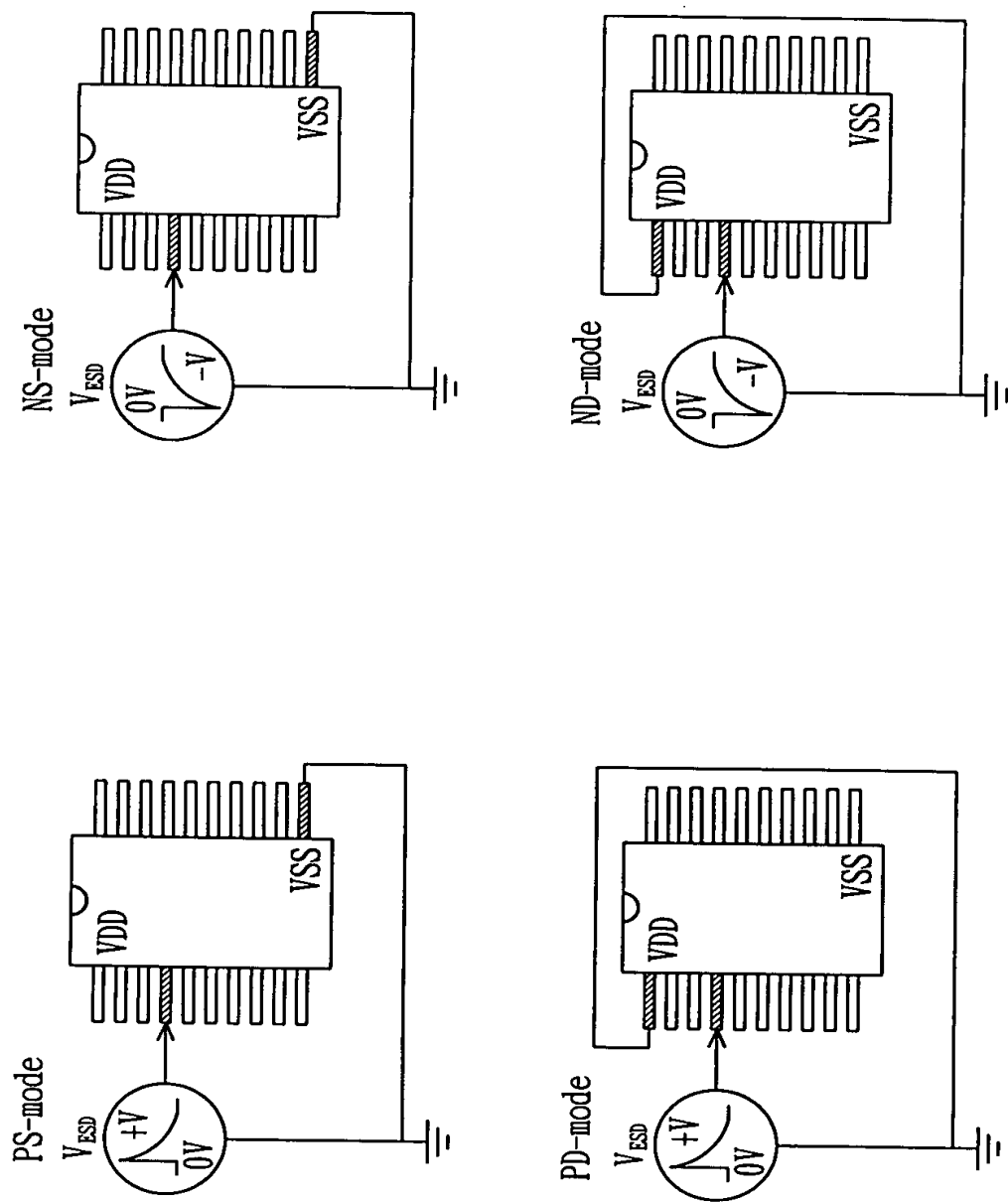


FIG. 4 (PRIOR ART)

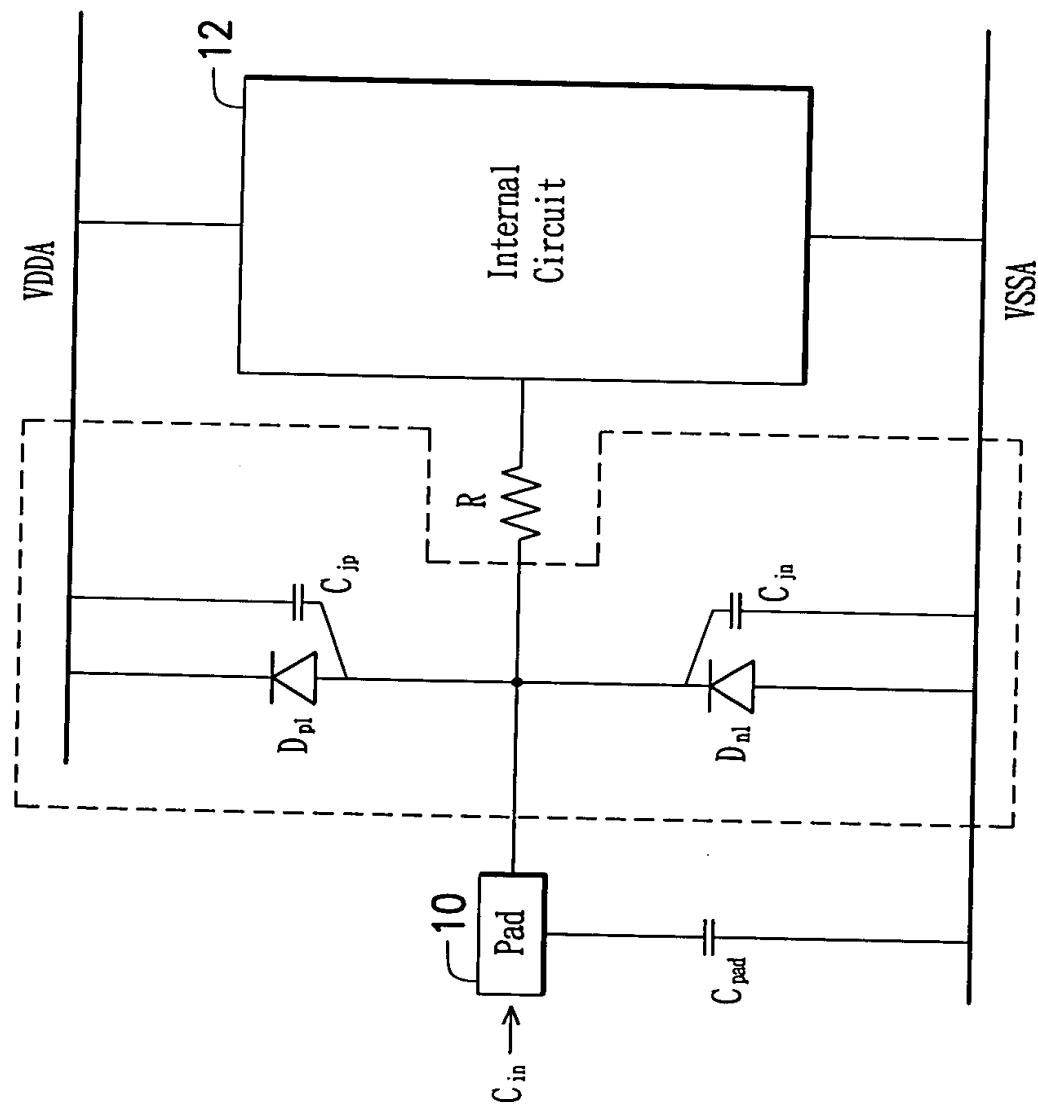


FIG. 5 (PRIOR ART)

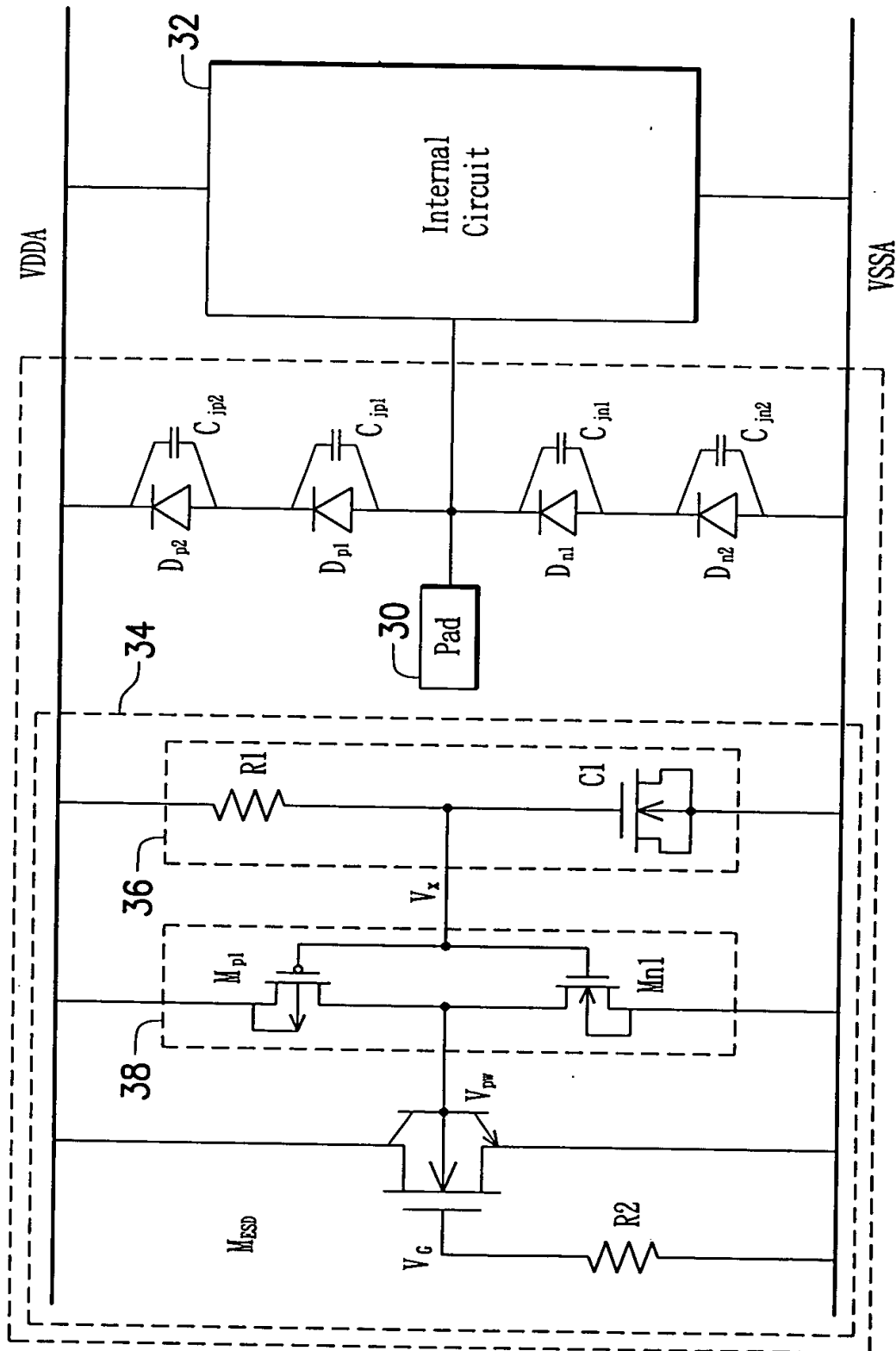


FIG. 6

FIG. 7

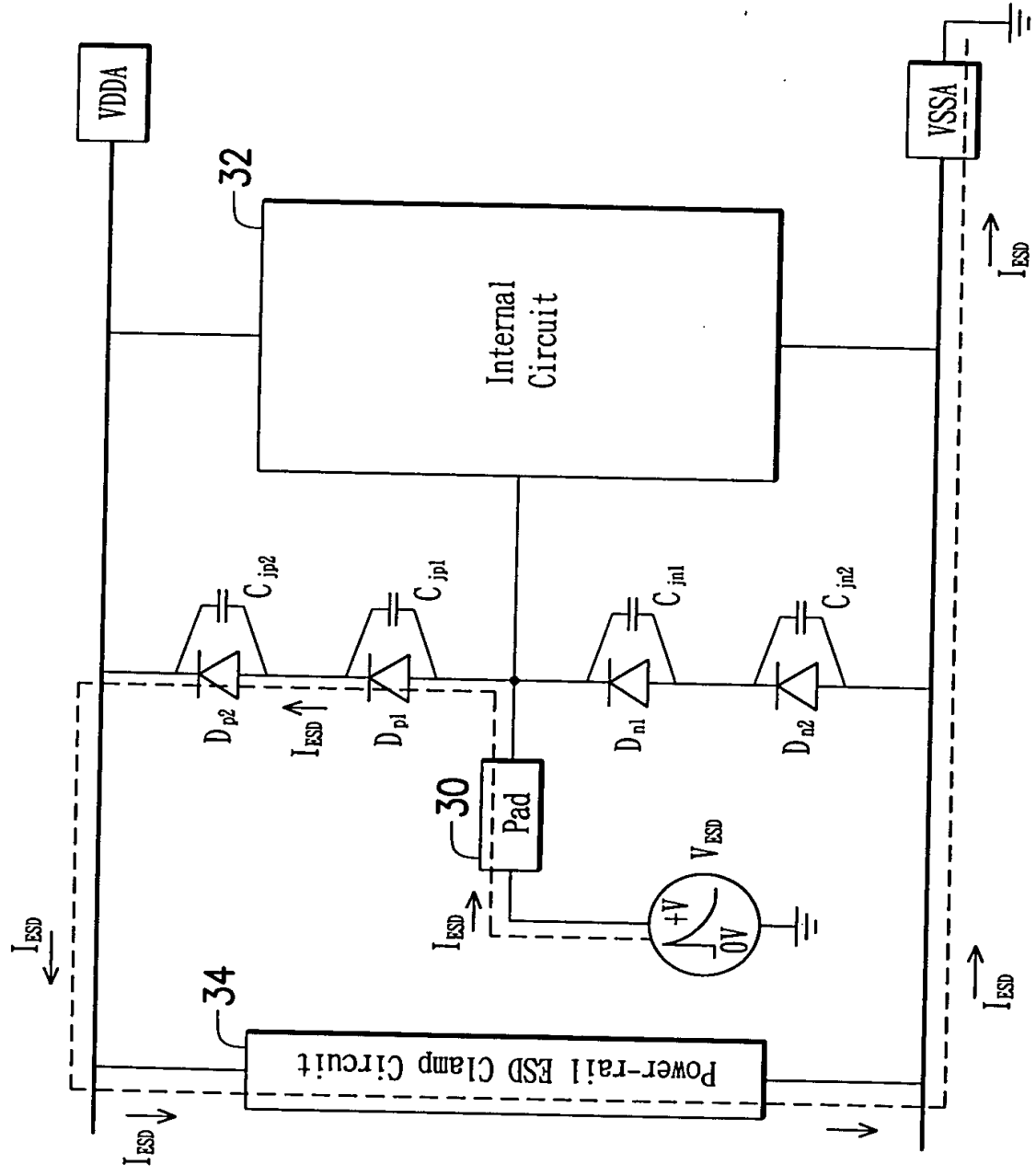


FIG. 7

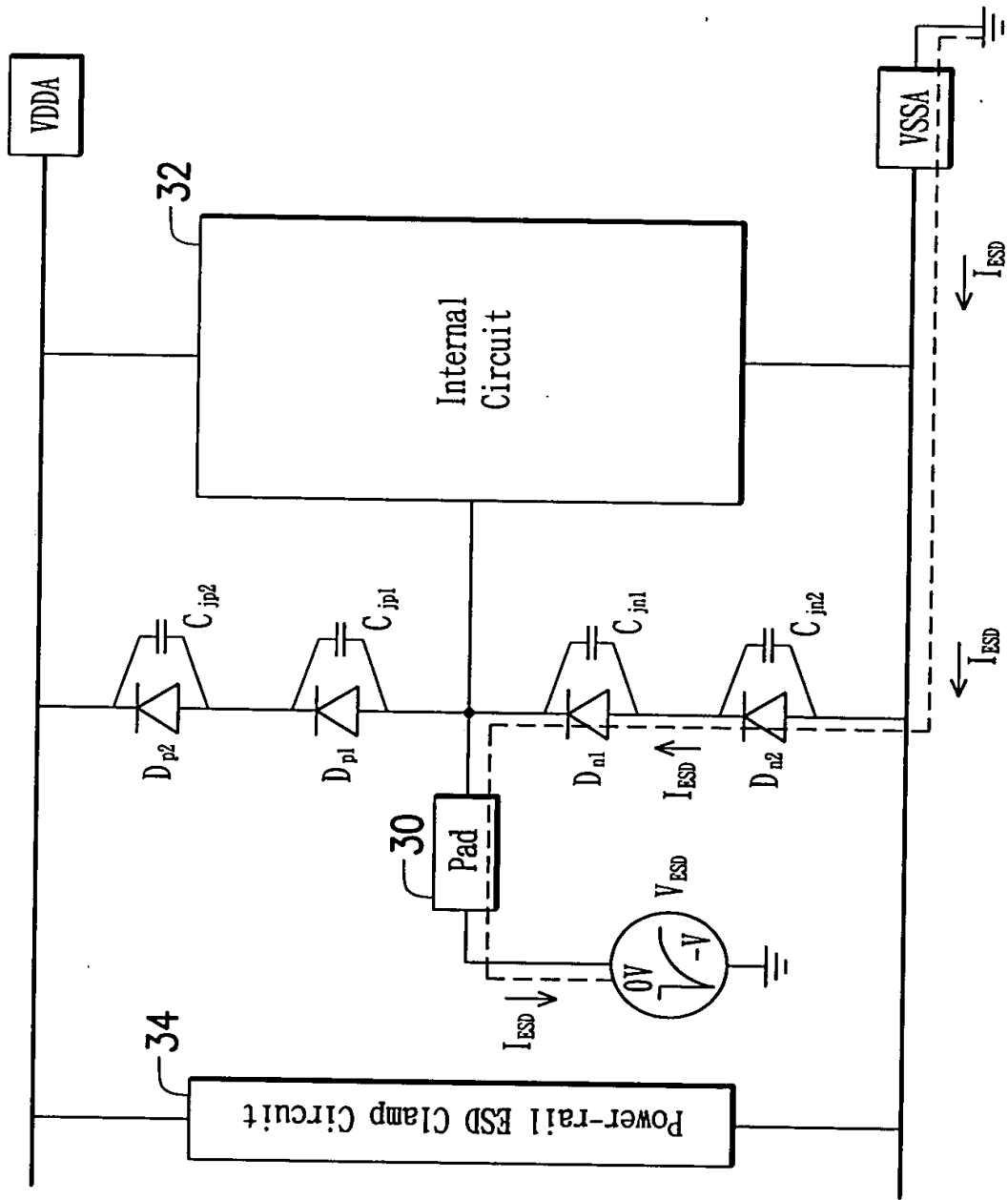


FIG. 8

FIG. 9 is a schematic diagram of an ESD protection circuit for a power rail. The circuit includes a Power-rail ESD Clamp Circuit (34) connected to VDDA and VSSA. An Internal Circuit (32) is also connected to VDDA and VSSA. A Pad (30) is connected to the Power-rail ESD Clamp Circuit (34) and the Internal Circuit (32). The Pad (30) is protected by a series of diodes and capacitors: D_{p2} and C_{jp2} are connected to VDDA; D_{p1} and C_{jp1} are connected to the Internal Circuit (32); D_{n1} and C_{jn1} are connected to the Internal Circuit (32); and D_{n2} and C_{jn2} are connected to VSSA. A voltage source V_{ESD} is applied to the Pad (30), and the resulting current I_{ESD} is shown flowing through the circuit.

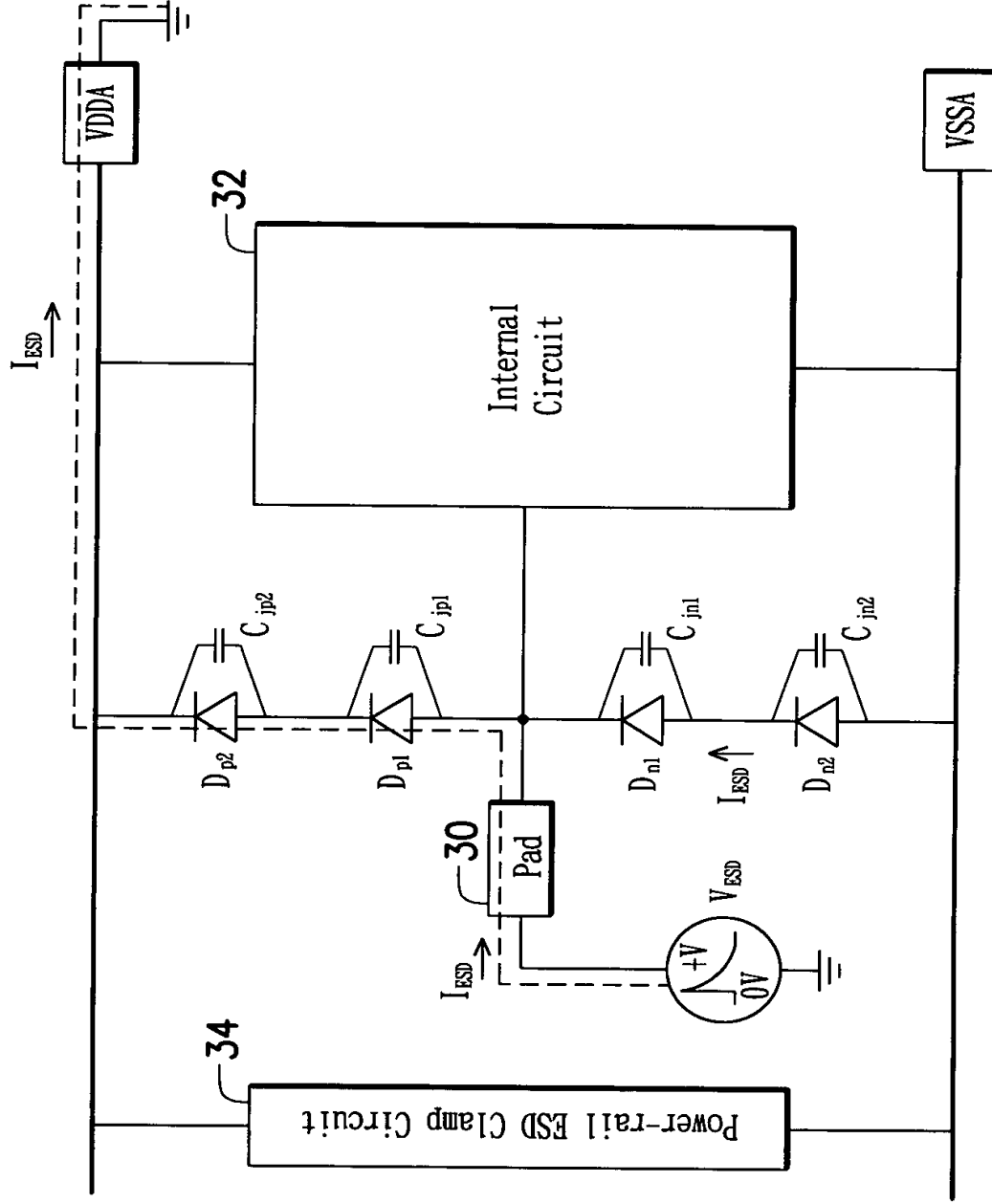


FIG. 9

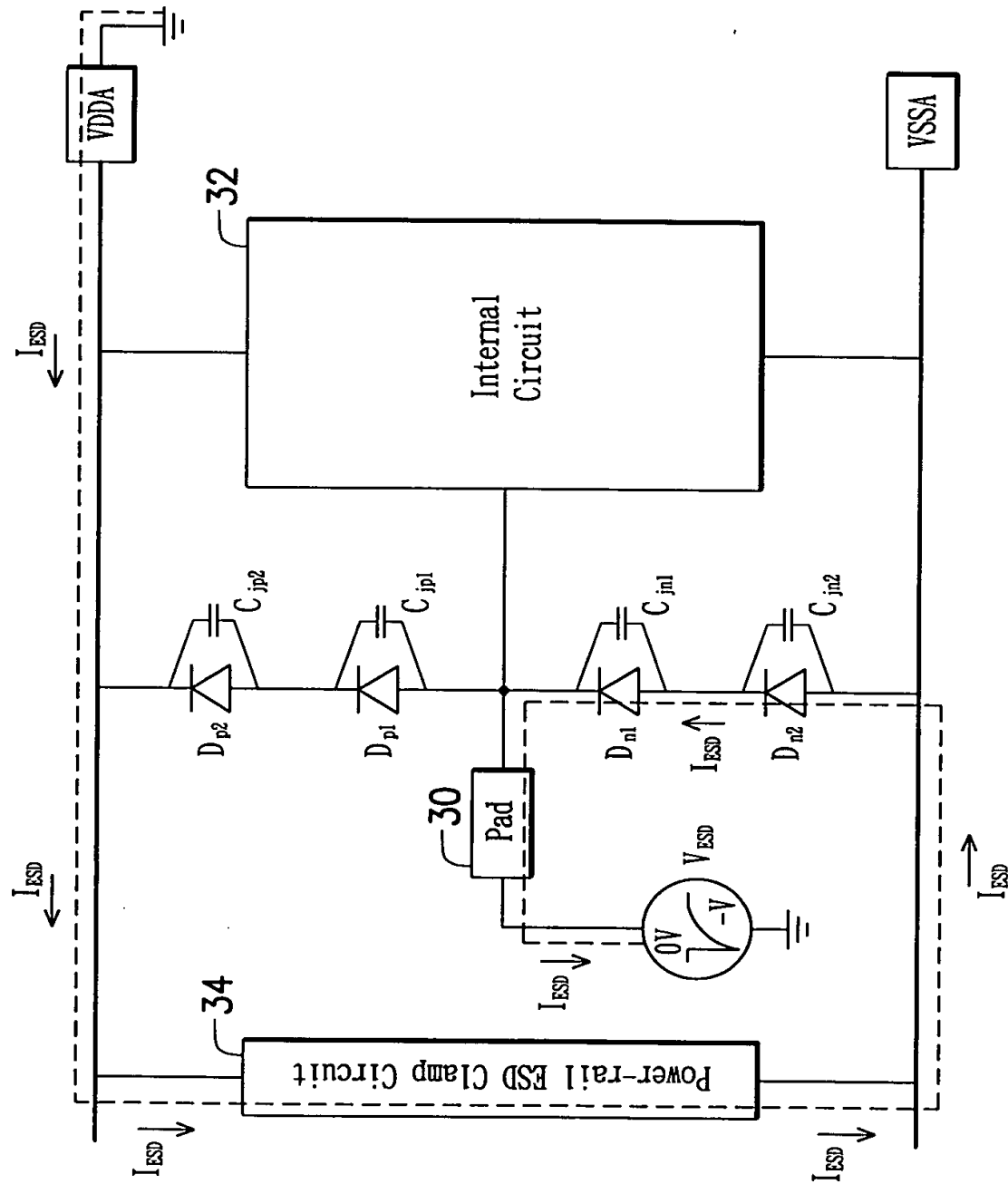


FIG. 10

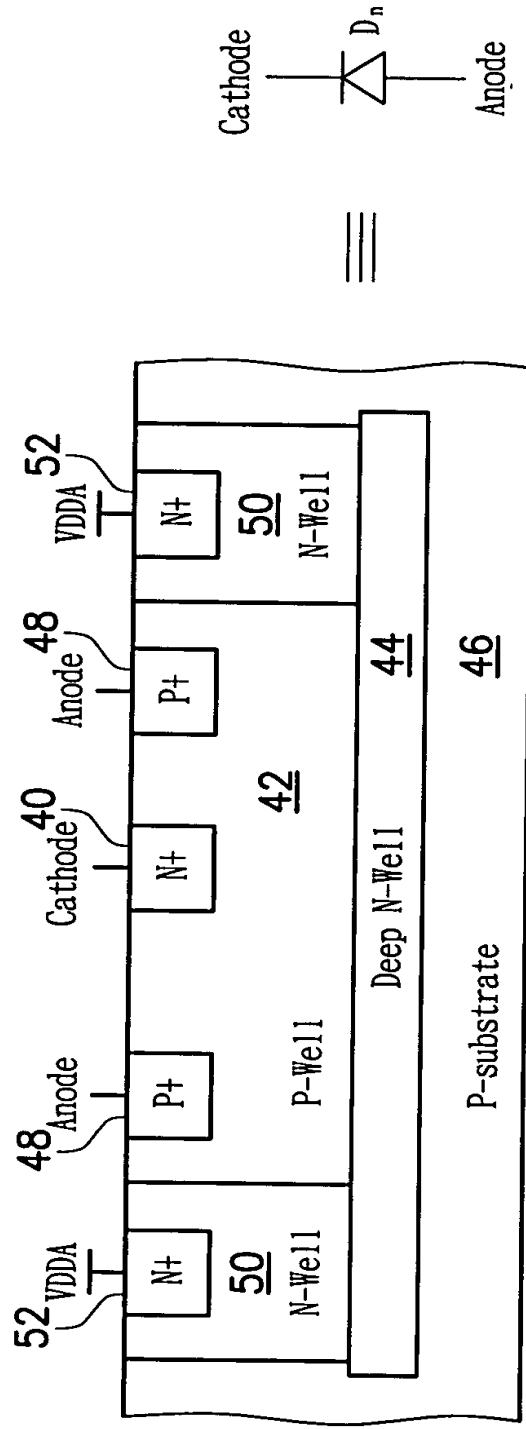


FIG. 11

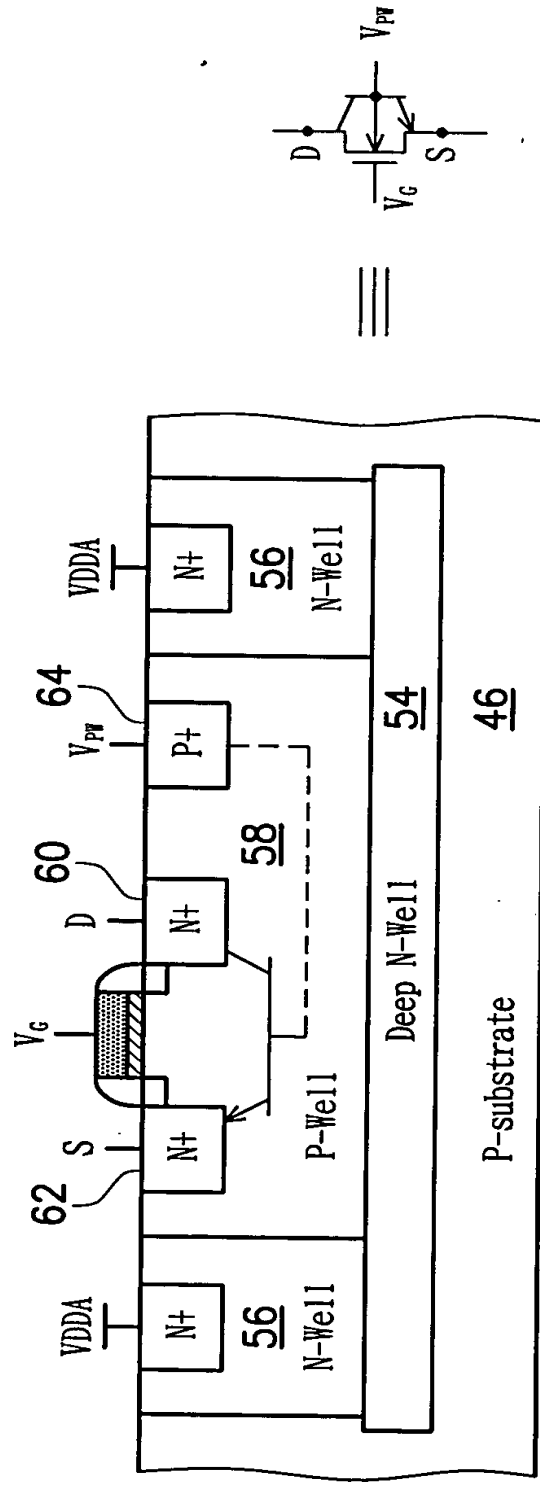


FIG. 12

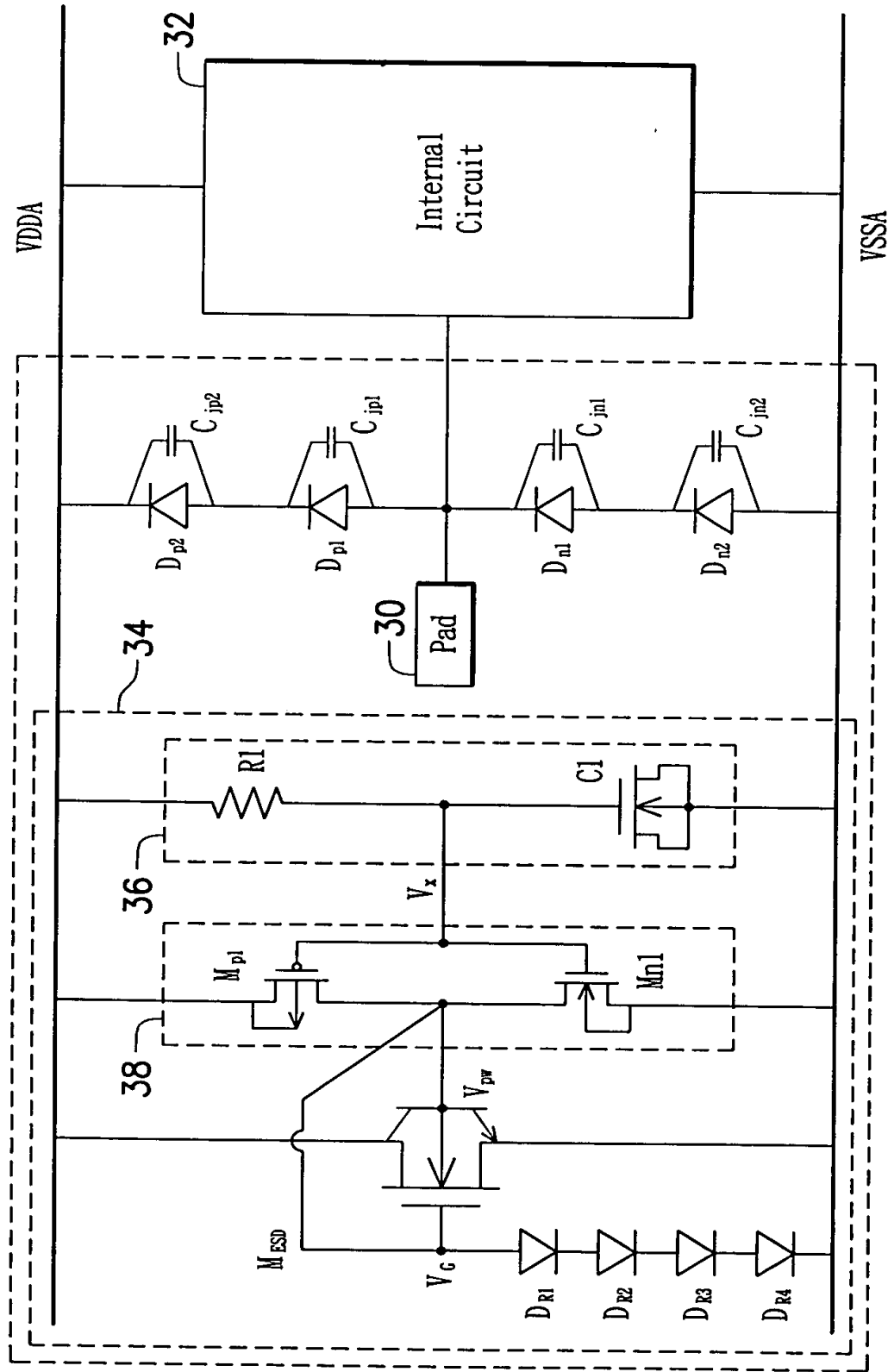


FIG. 13

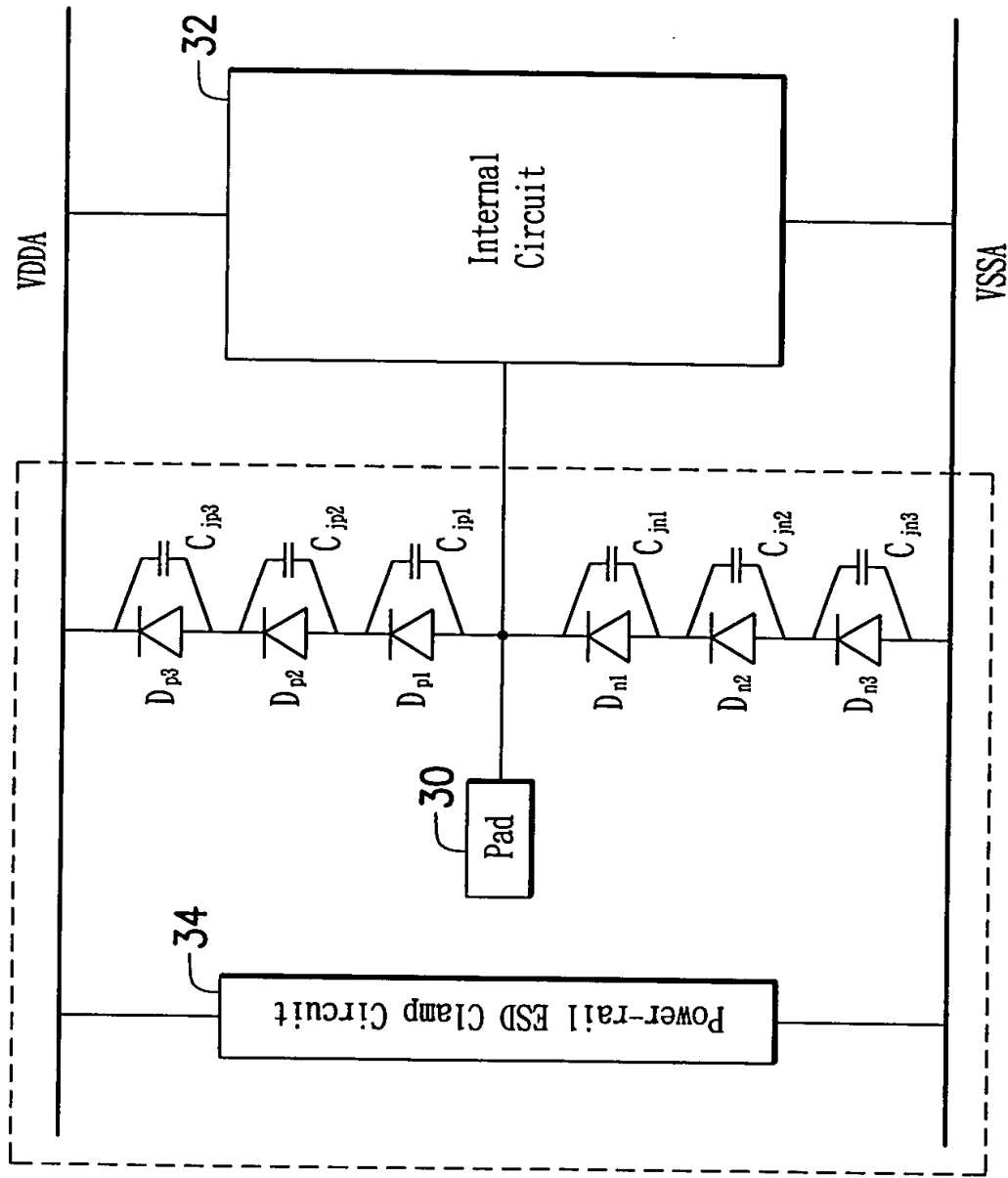


FIG. 14

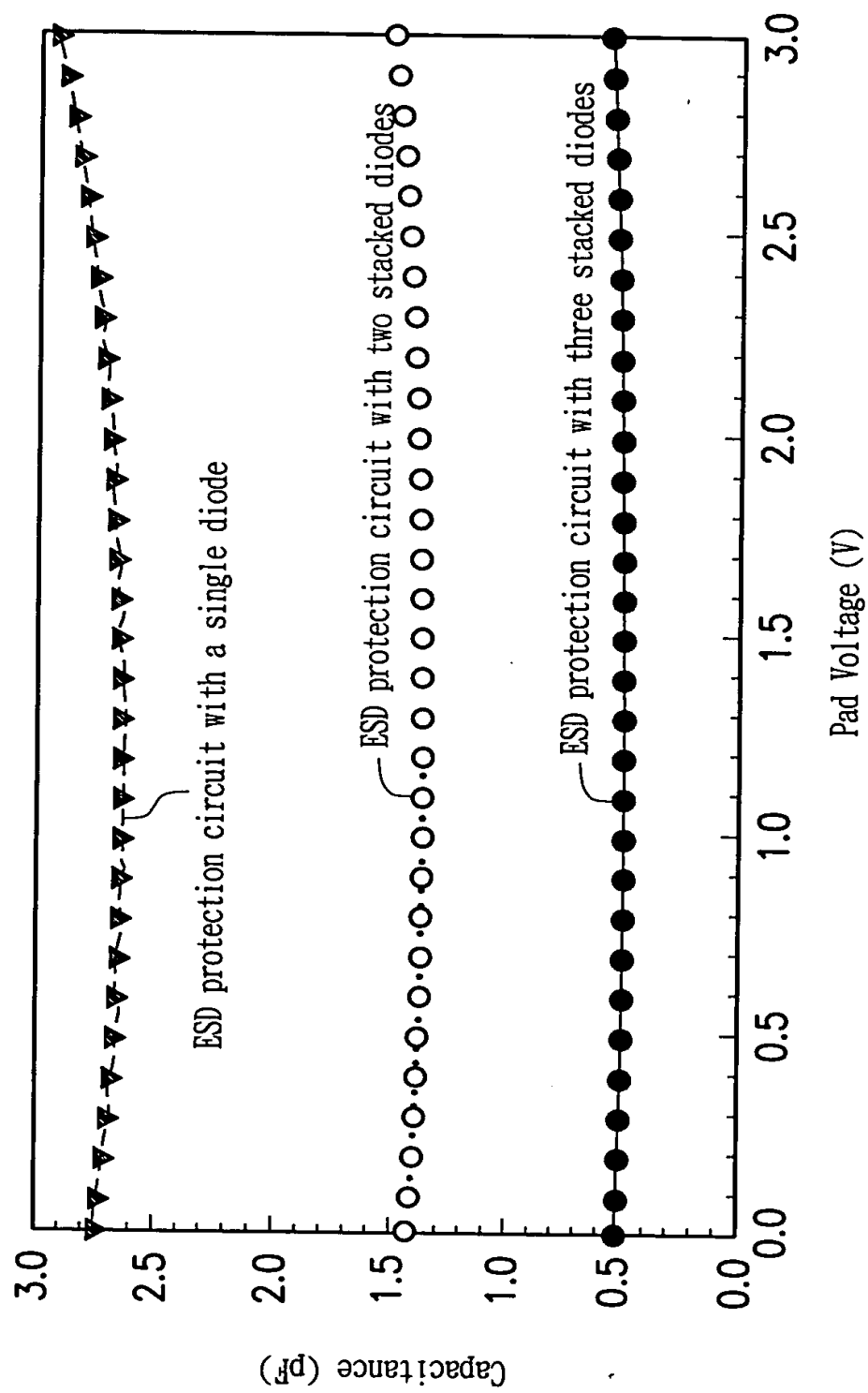


FIG. 15

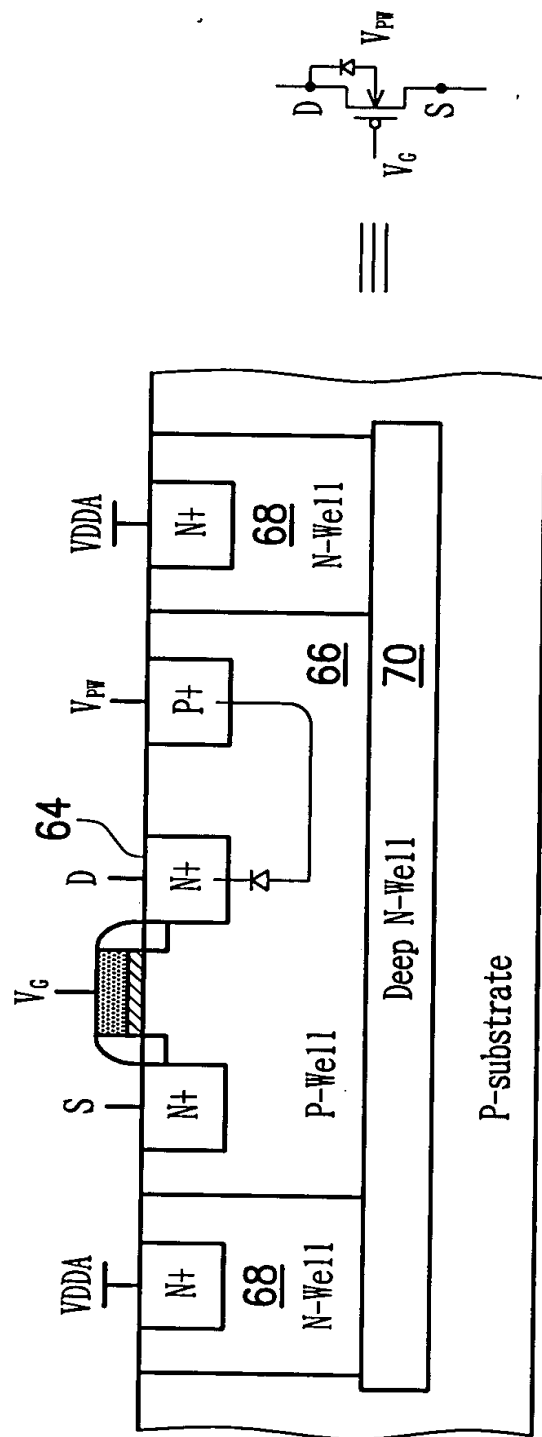


FIG. 16

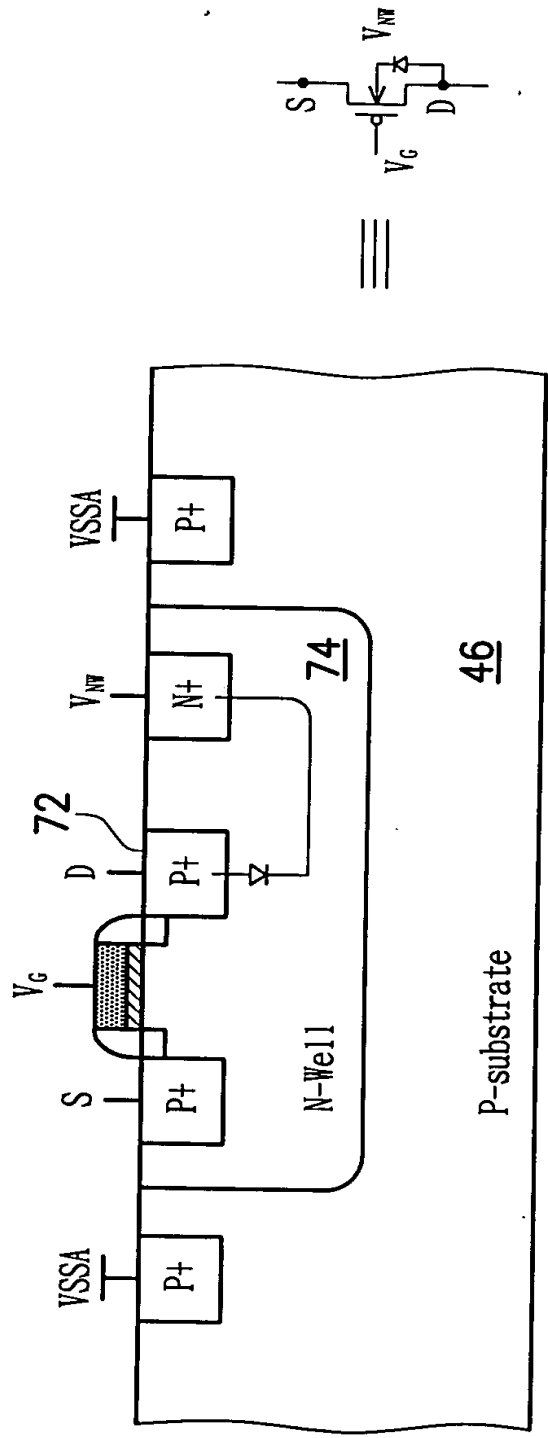


FIG. 17

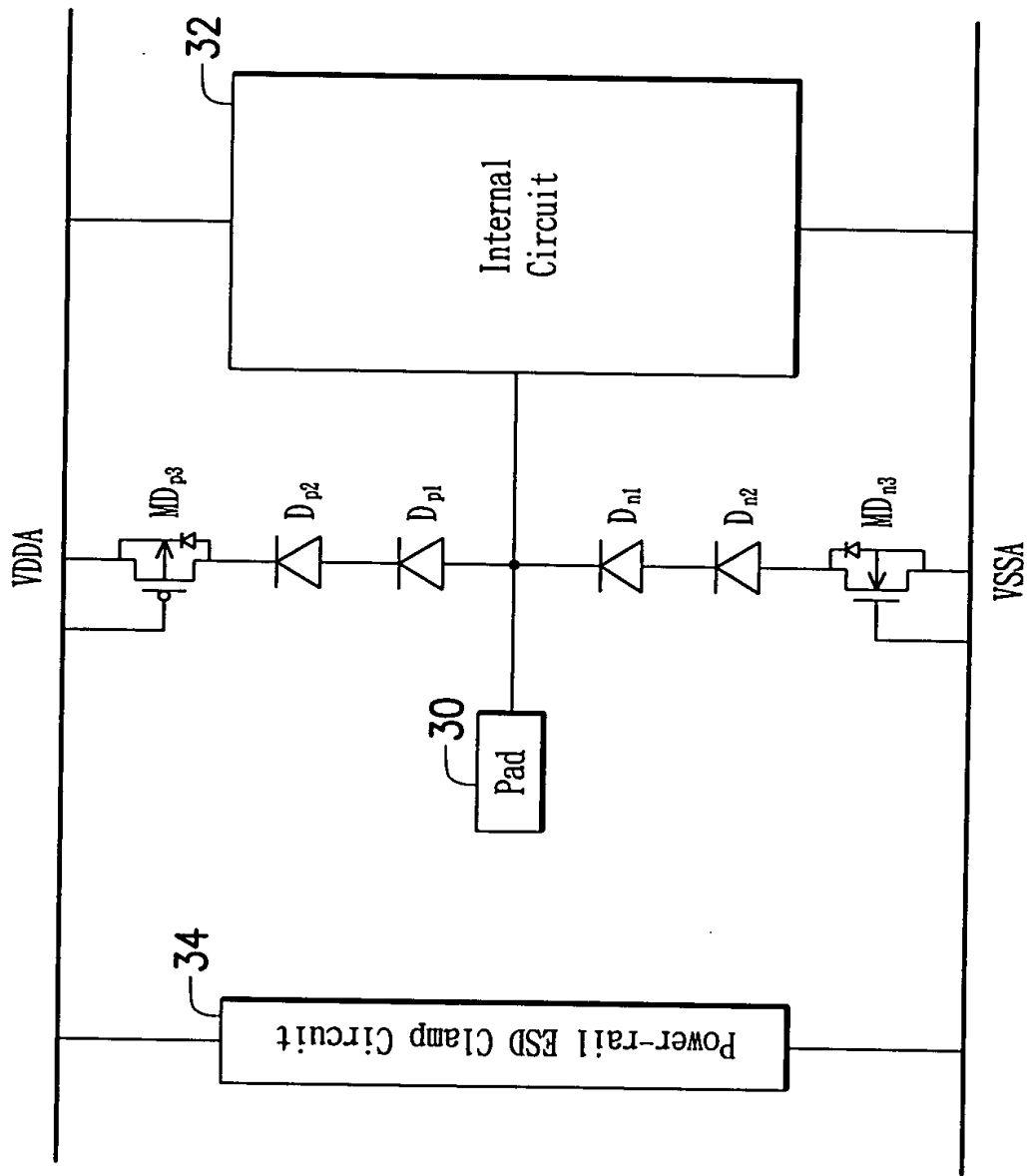


FIG. 18

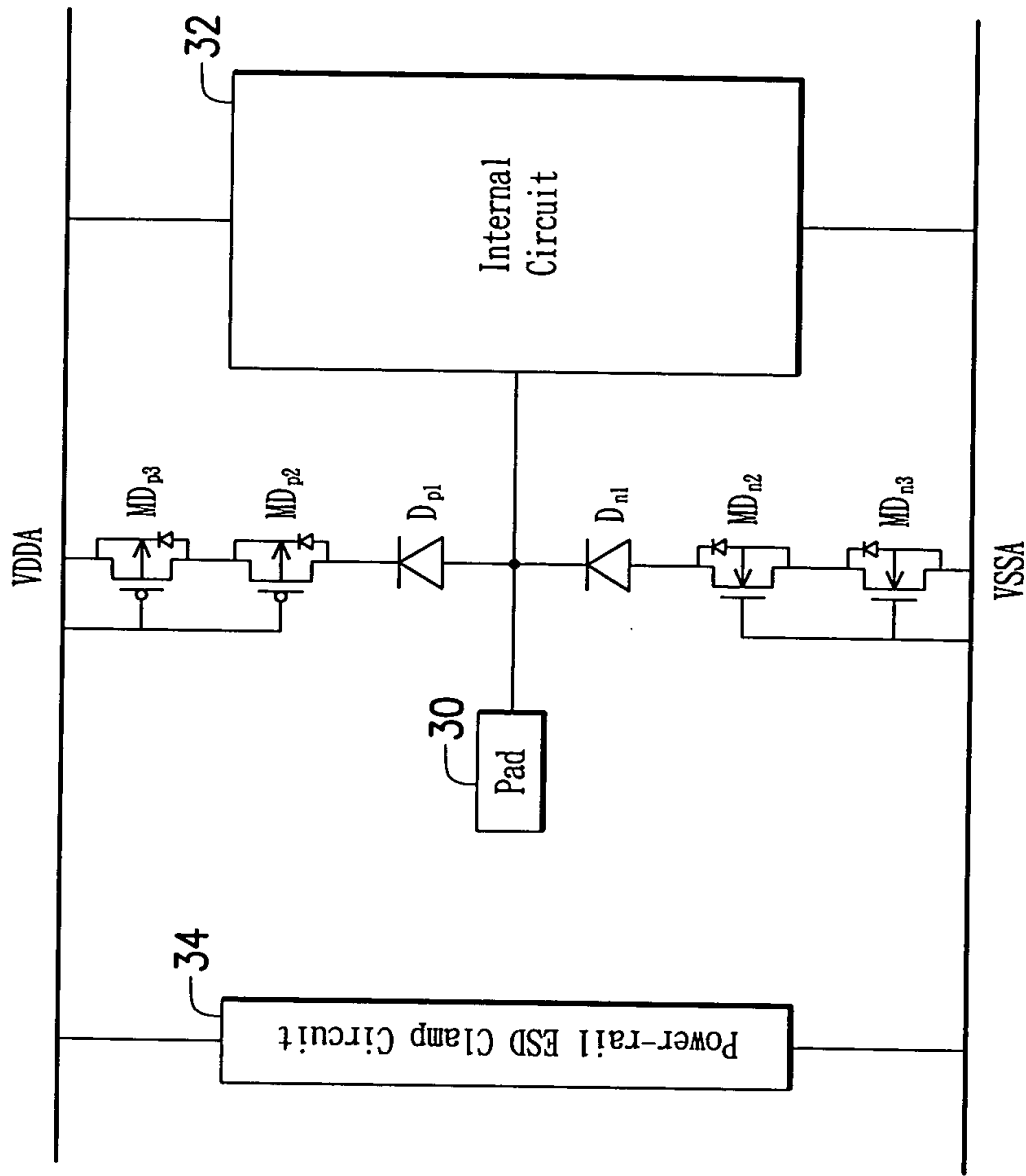


FIG. 19

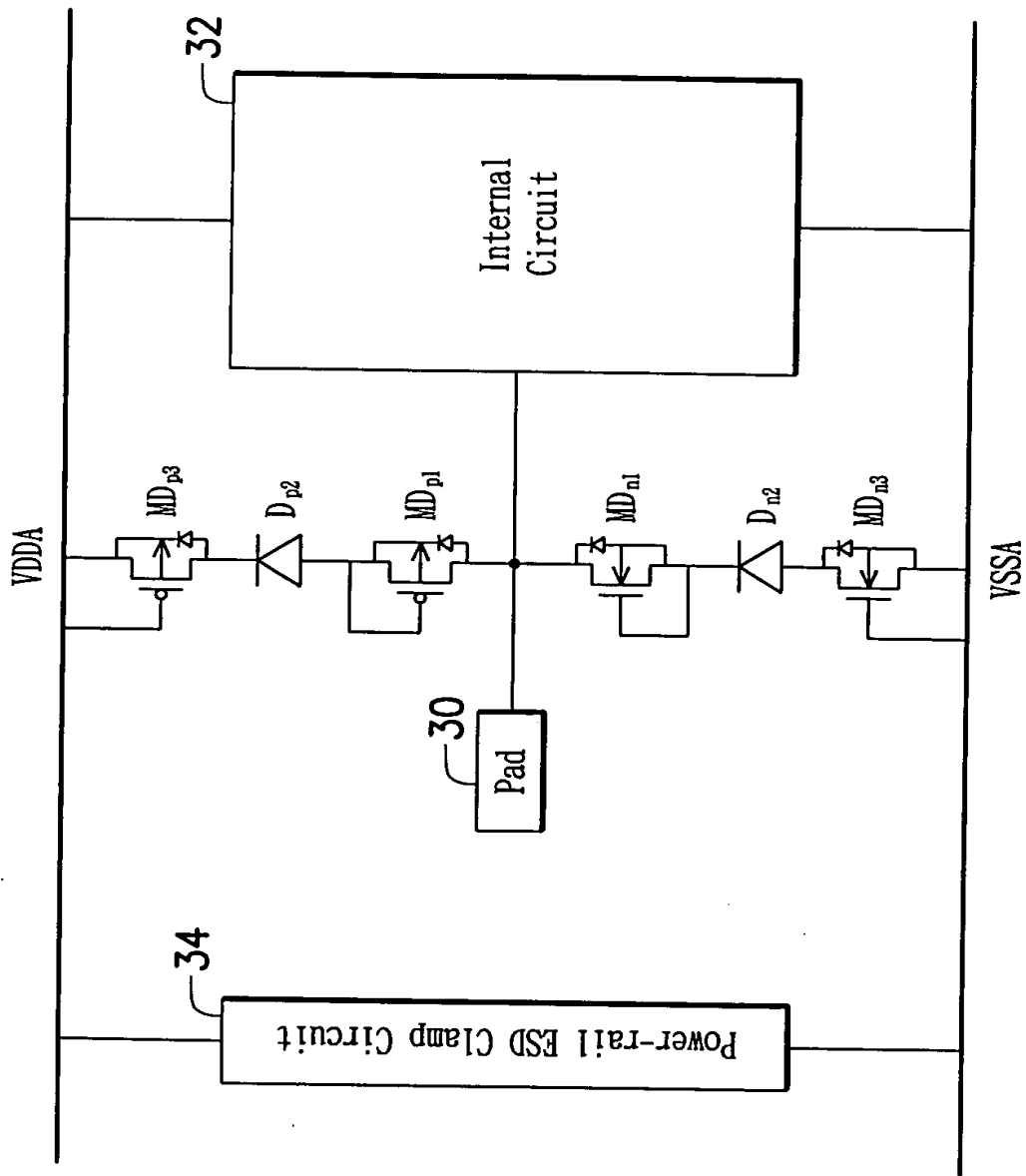


FIG. 20

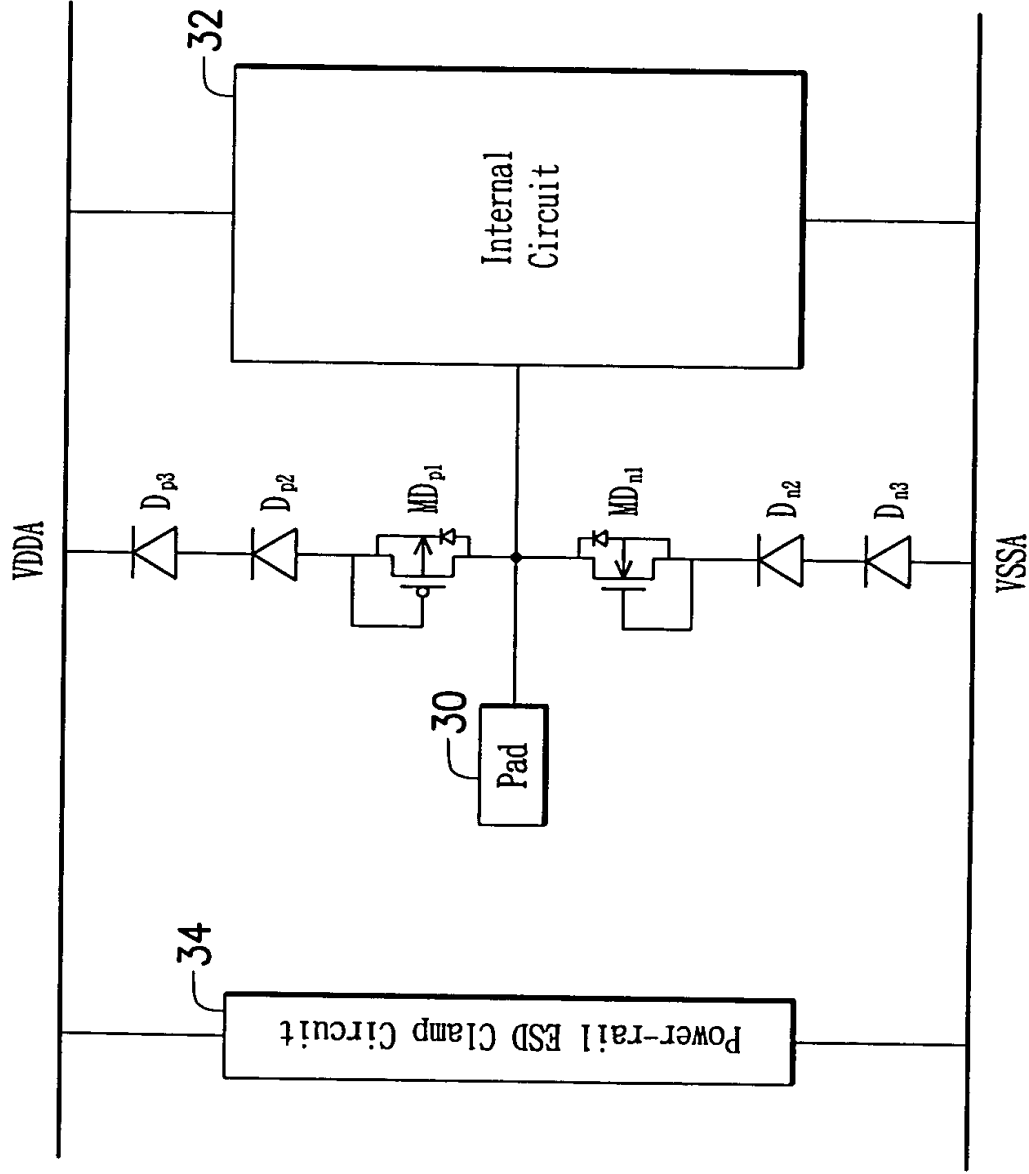


FIG. 21

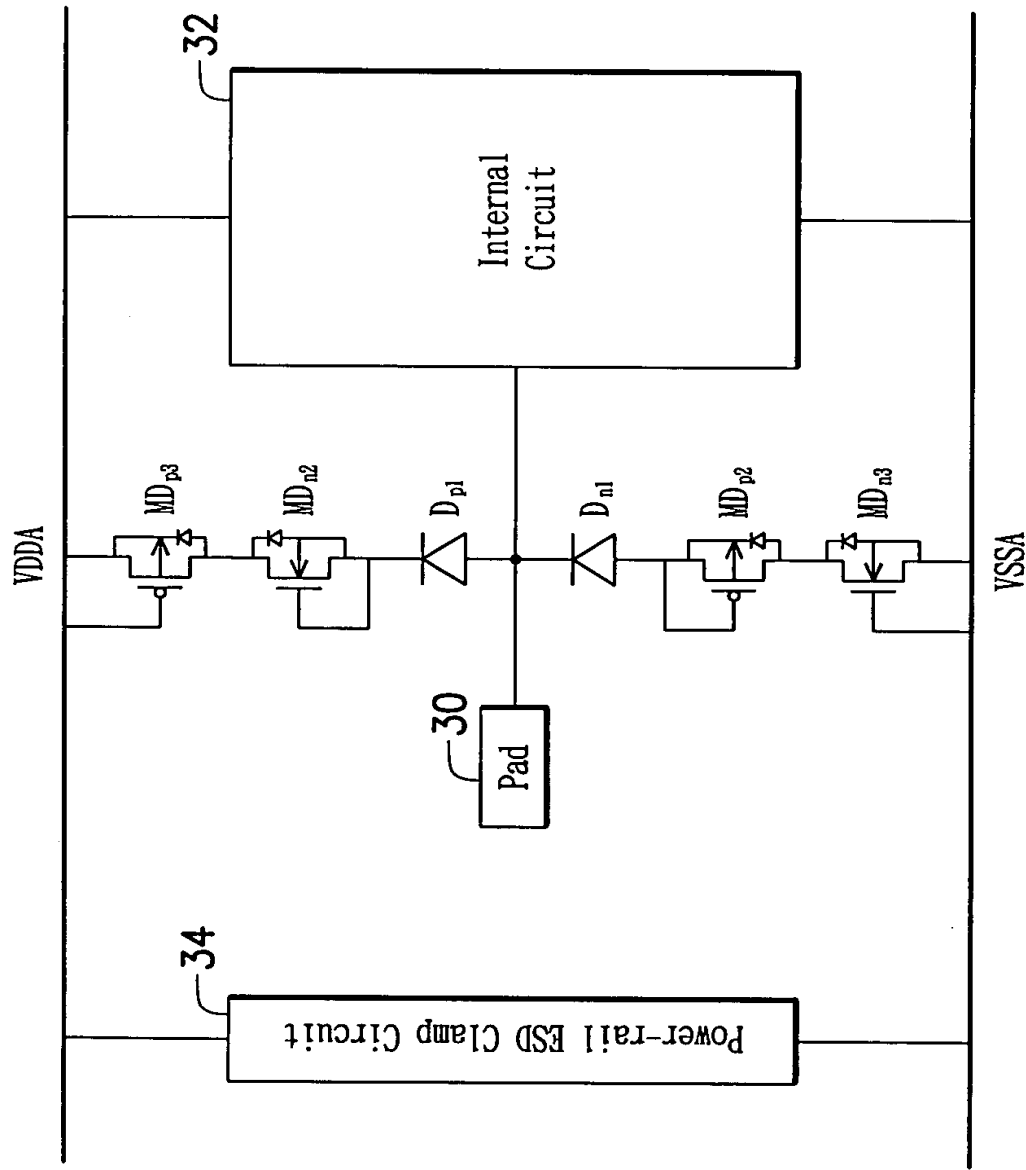


FIG. 22

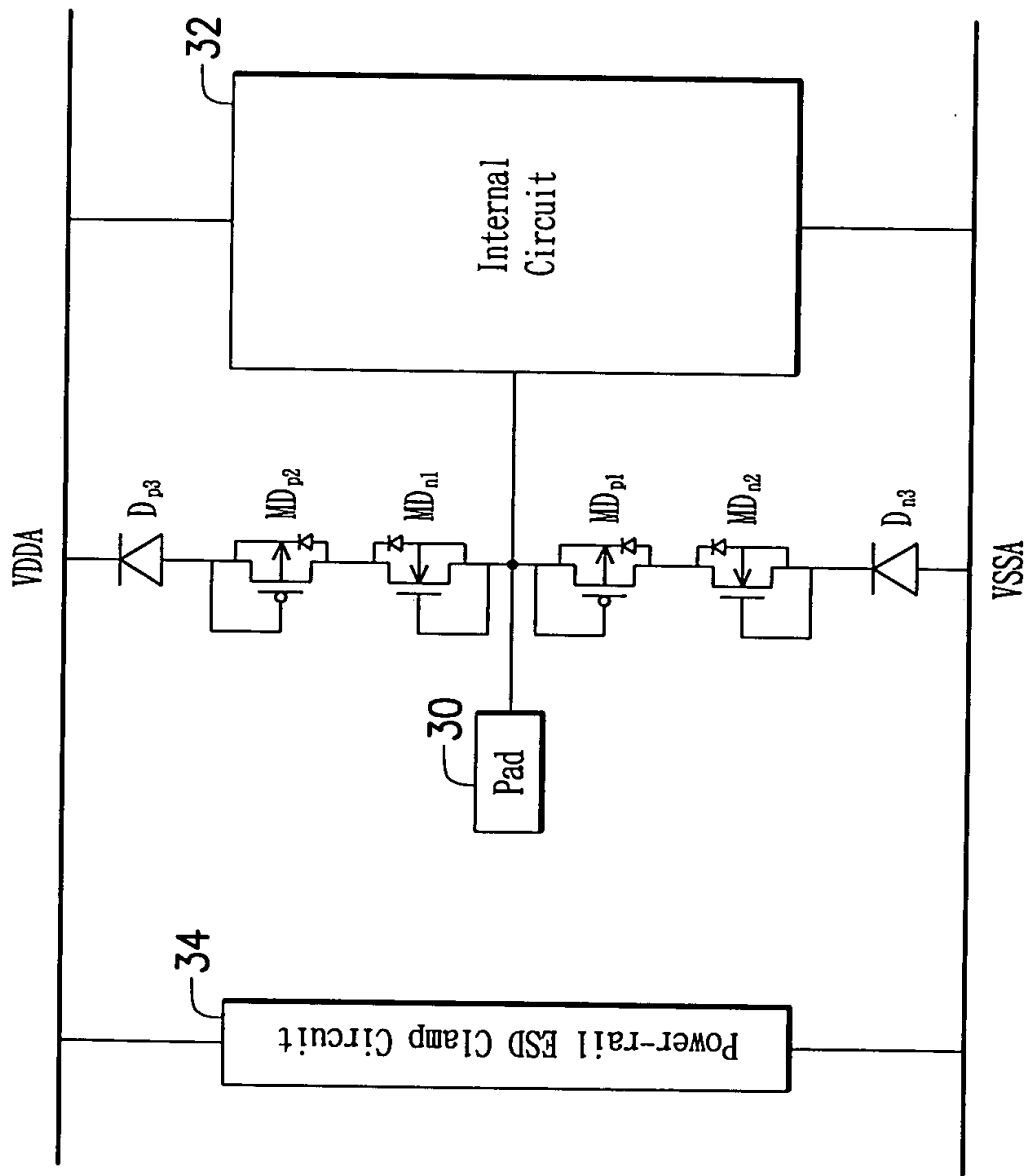


FIG. 23

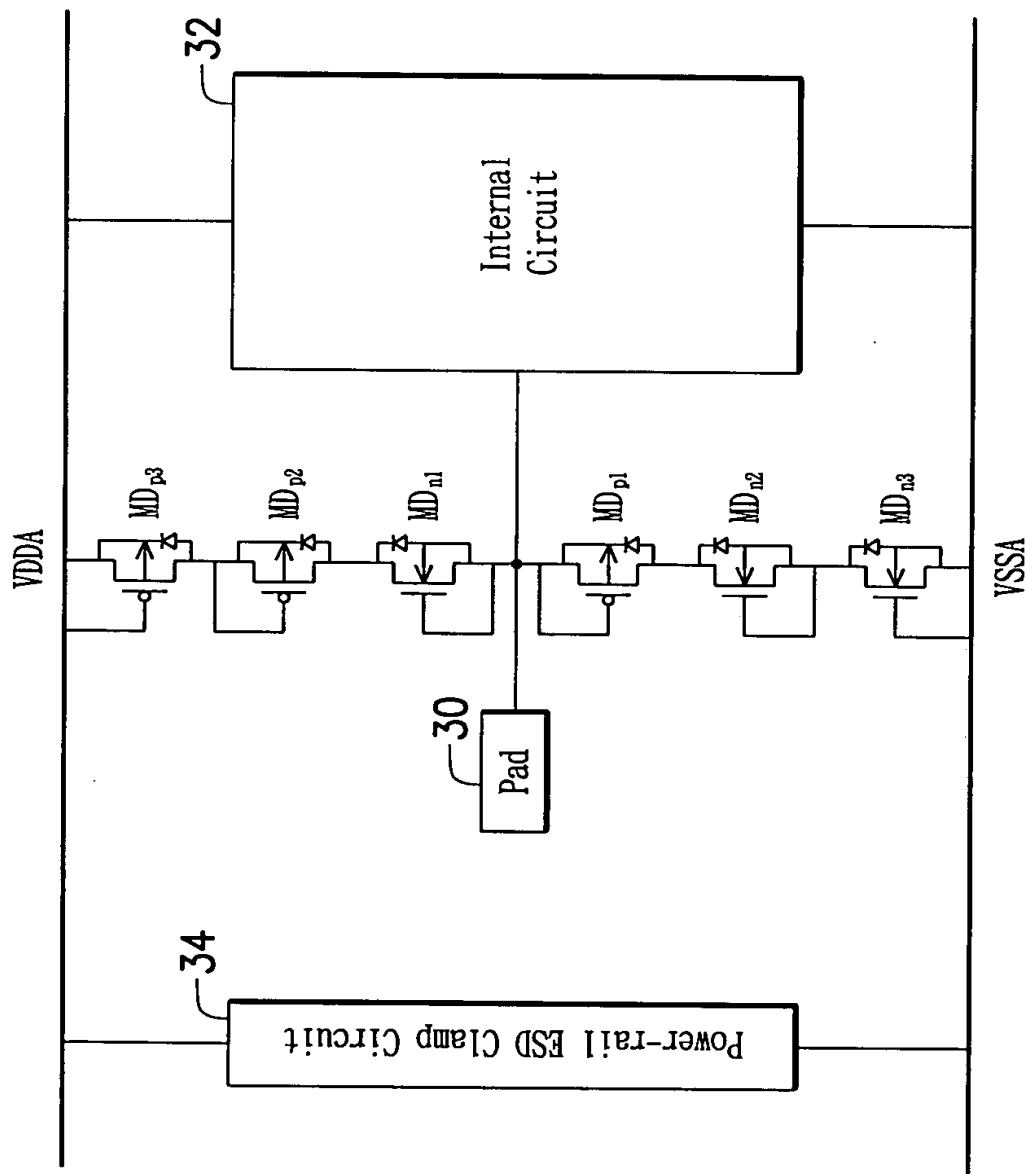


FIG. 24

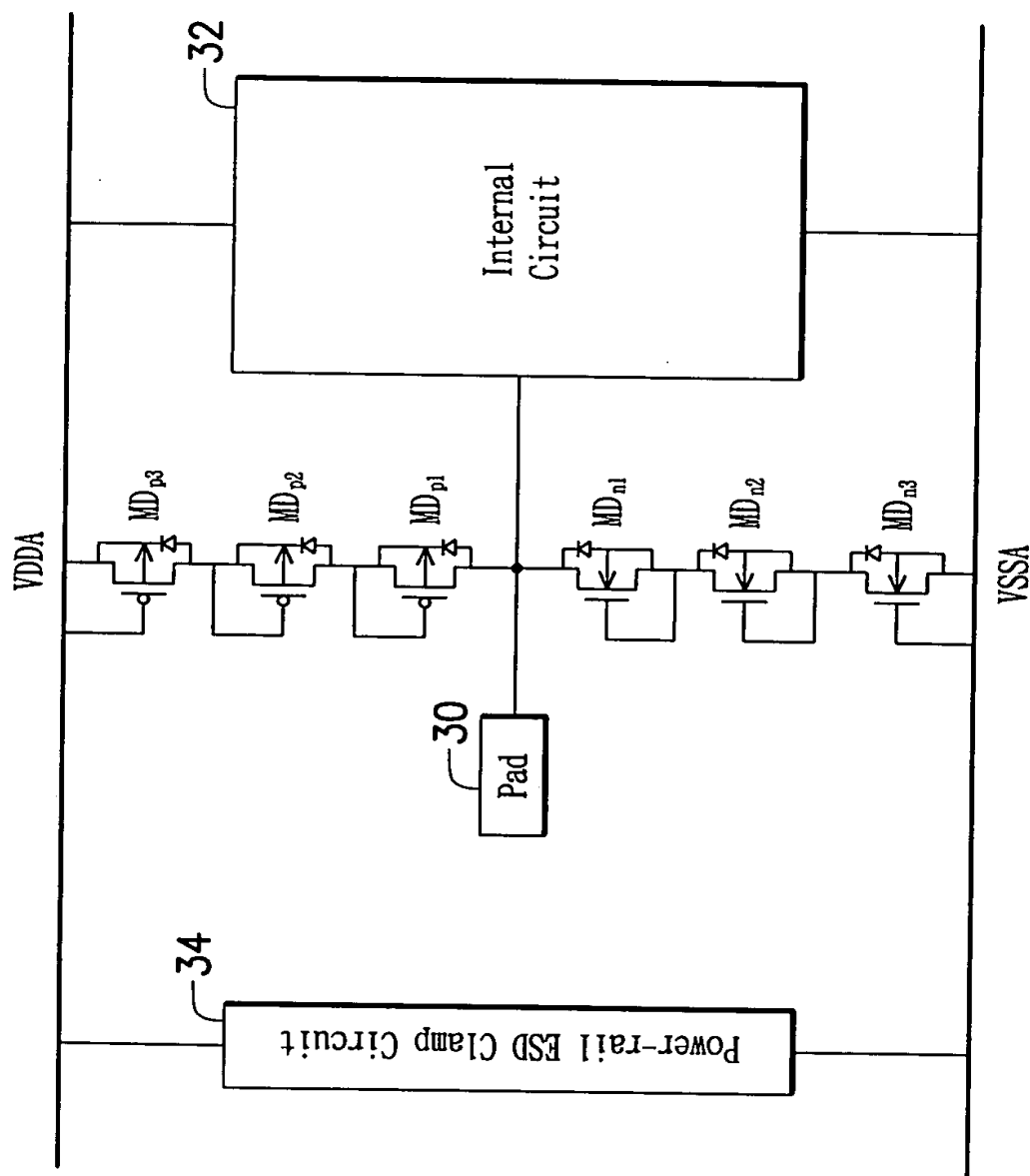


FIG. 25